CCS Technical Documentation
NPD-4 Series Transceivers

System Module

Issue 1 02/2003 Confidential

Contents

Transceiver NPD-4

Introduction

The NPD-4 is available as a CDMA tri-mode engine (1900/800 MHz CDMA and 800 MHz AMPS), supporting the new CDMA 1XRTT standard air interface.

Advanced messaging features include SMS, (MO/MT), Instant Messaging, Nokia 'Chat' and Smart Messaging (ring tones, MIDI sound support, graphics, images, and animations). Global Positioning System (GPS) technology is supported.

The standard internal battery (BLC-2) provides users with up to 3:45 hours of talk time (digital) and 1:45 hours of talk time (analog). Standby time is 235 hours (digital) and 25 hours (analog).

The transceiver has a full graphic display and the user interface is based on the Jack 3.4 (Series 30) UI with 4-way scroll keys.

Three antennas are used — internal; external, extendable silver "whip"; and GPS. When the whip antenna is in, only the internal antenna is active. When the whip is retracted, both antennas are active. Access to test the cellular engine is possible once the A cover is removed. A second RF connector to test GPS technology is possible via removal of the B cover.

Operational Modes

There are several different operational modes: Modes have different states controlled by the cellular SW. Some examples are: Idle State (on ACCH), Camping (on DCCH), Scanning, Conversation, No Service Power Save (NSPS) *previously OOR = Out of Range*.

In the power-off mode, only the circuits needed for power-up are supplied.

In the idle mode, circuits are powered down and only the sleep clock is running.

In the active mode, all the circuits are supplied with power, although some parts might be in idle state part of the time.

The charge mode is effective in parallel with all previous modes. The charge mode itself consists of two different states, *i.e.* the fast charge and the maintenance mode.

The local mode is used for alignment and testing.

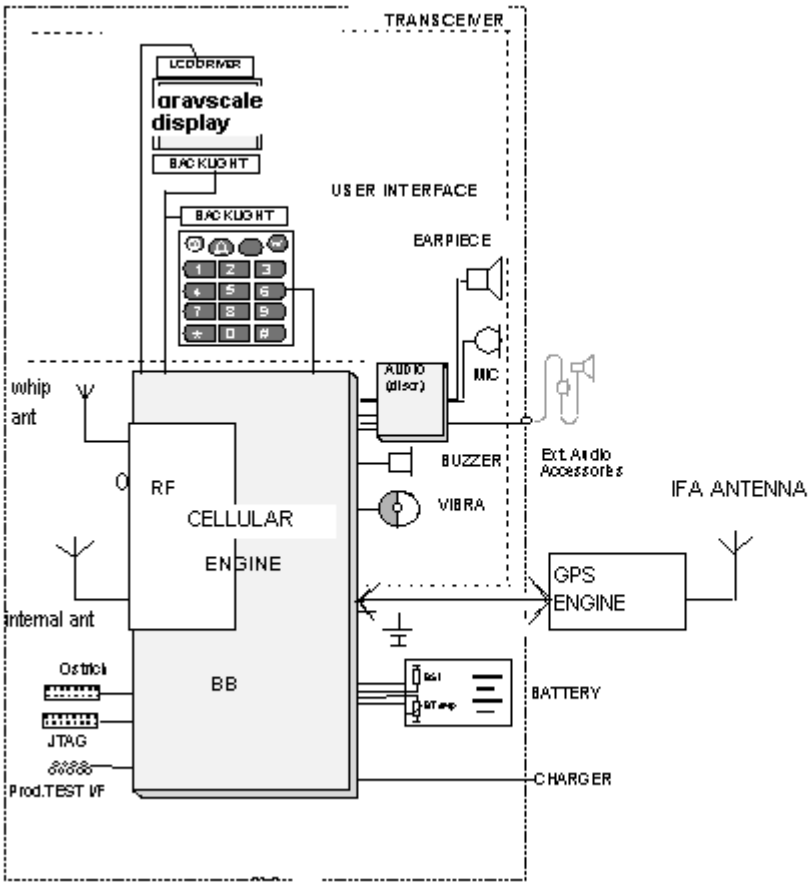


Figure 1: Interconnecting Diagram

Engine Module

Environmental Specifications

Normal and extreme voltages

Voltage range:

- nominal battery voltage: 3.6 V
- maximum battery voltage: 4.5 V
- minimum battery voltage: 3.2 V

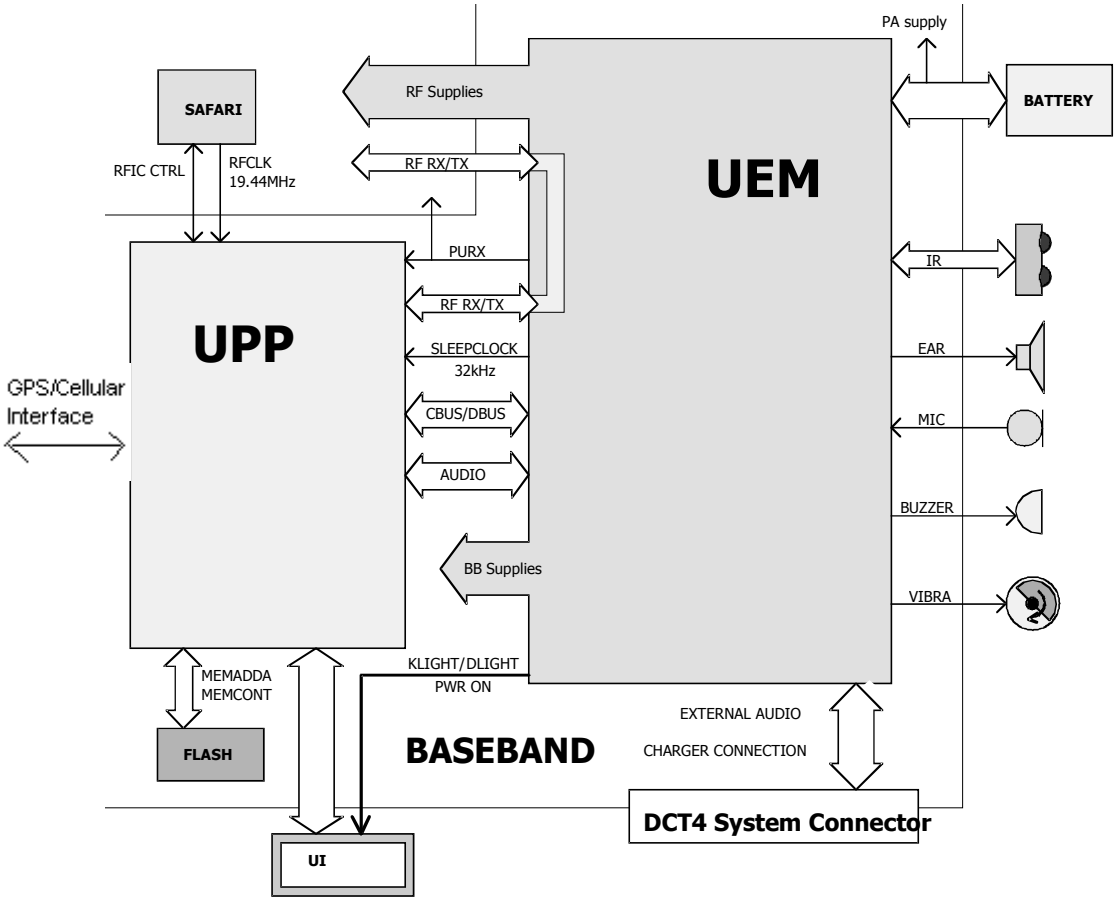
Temperature Conditions

Temperature range:

- ambient temperature: -30...+ 60^{o} C
- PWB temperature: -30...+85^{o} C

Baseband Module

The core part of the NPD-4 baseband module consists of two ASICs — UEM and UPP — and flash memory. The following sections describe these parts.



UEM

UEM Introduction

UEM is the Universal Energy Management IC for DCT4 digital handportable phones. In addition to energy management, it performs all the baseband mixed-signal functions.

Most of UEM pins have 2kV ESD protection. Those signals that are considered to be exposed more easily to ESD have 8kV protection inside UEM. Such signals are all audio signals, headset signals, BSI, Btemp, Fbus, and Mbus signals.

Regulators

UEM has six regulators for baseband power supplies and seven regulators for RF power supplies. VR1 regulator has two outputs VR1a and VR1b. NPD-1 has a DC/DC connector to provide power to the UPP VCORE.

Bypass capacitor (1uF) is required for each regulator output to ensure stability.

Reference voltages for regulators require external 1uF capacitors. Vref25RF is reference voltage for VR2 regulator; Vref25BB is reference voltage for VANA, VFLASH1, VFLASH2,

VR1 regulators; Vref278 is reference voltage for VR3, VR4, VR5, VR6, VR7 regulators; VrefRF01 is reference voltage for VIO, VCORE, VSIM regulators, and for RF.

BB	RF
VANA: 2.78Vtyp 80mAmax	VR1a:4.75V 12mAmax VR1b:4.75V 12mAmax
Vflash1: 2.78Vtyp 70mAmax	
Vflash2: 2.78Vtyp 40mAmax	VR2:2.78V 100mAmax
VSim: 1.8/3.0V 25mAmax	VR3:2.78V 20mA
VIO: 1.8Vtyp 150mAmax	VR4: 2.78V 50mAmax
Vcore: 1.0-1.8V 200mAmax	VR5: 2.78V 50mAmax
	VR6: 2.78V 50mAmax
	VR7: 2.78V 45mAmax

VANA regulator supplies internal and external analog circuitry of BB. It is disabled in sleep mode.

Vflash1 regulator supplies LCD and digital parts of UEM ASIC. It is enabled during startup and goes to low Iq-mode in sleep mode.

Vflash2 regulator supplies data cable (DLR-3). It is enabled/disenabled through writing register and default is off.

VIO regulator supplies both external and internal logic circuitries. It is used by LCD, flash, Robin, Batman, GPS RF and GPS Baseband, and UPP. Regulator goes in to low Iq-mode in sleep mode.

VCORE DC/DC regulator supplies DSP, Core part of UPP, and GPS Baseband ASIC. Voltage is programmable and the startup default is 1.5V. Regulator goes to low Iq-mode in sleep mode.

VR1 regulator uses two LDOs and a charge pump. This regulator is used by Robin RF ASIC (VR1B) and synthesizer circuits (VR1A).

VR2 is a linear regulator used to supply Robin RF ASIC and the detector circuitry.

VR3 is a linear regulator used by Robin RF ASIC and VCTCXO circuitry.

VR4 is a linear regulator used by the PLL and UHF VCO circuitry.

VR5 is a linear regulator used by the Batman RFIC and the Alfred RF ASIC.

VR6 is a linear regulator used by Robin RF ASIC and TX LO buffer.

VR7 is a linear regulator used by Batman RF ASIC.

IPA1 and IPA2 are programmable current generators. The 27kW/1%/100ppm external resistor is used to improve the accuracy of output current. IPA1 is used by lower band PA and IPA2 is used by higher band PA.

RF Interface

UEM handles the interface between the baseband and the RF section. It provides A/D and D/A conversion of the in-phase and quadrature receive and transmit signal paths, and also A/D and D/A conversions of received and transmitted audio signals to and from the UI section. The UEM supplies the analog AFC signal to the RF section according to the UPP DSP digital control. It also converts PA temperature into real data for the DSP.

Charging Control

The CHACON block of UEM asics controls charging. Needed functions for charging controls are pwm-controlled battery charging switch, charger-monitoring circuitry, battery voltage monitoring circuitry and RTC supply circuitry for backup battery charging. In addition, external components are needed for EMC protection of the charger input to the baseband module. The DCT4 baseband is designed to electrically support both DCT3 and DCT4 chargers.

Digital Interface

Data transmission between the UEM and the UPP is implemented using two serial connections, DBUS (9.6 MHz) for DSP and CBUS (1.2 MHz in CDMA) for MCU. UEM is a dual-voltage circuit: the digital parts are running from 1.8V and the analog parts are running from 2.78V. Vbat (3,6V) voltage regulators inputs also are used.

Audio Codec

The baseband supports two external microphone inputs and one external earphone output. The inputs can be taken from an internal microphone, from a headset microphone, or from an external microphone signal source through a headset connector. The output for the internal earpiece is a dual-ended type output, and the differential output is capable of driving 4Vpp to the earpiece with a 60 dB minimum signal to total distortion ratio. Input and output signal source selection and gain control is performed inside the UEM ASIC according to control messages from the UPP. Both a buzzer and an external vibra alert control signals are generated by the UEM with separate PWM outputs.

MIDI

The MIDI audio signal generated by the DSP and UEM audio CoDec is routed to the XEAR output of the UEM. An audio amplifier (LM4890) is used to boost enough power for the speaker.

UI Drivers

There is a single output driver for vibra, display, and keyboard LEDs inside UEM. These generate PWM square wave to devices.

AD Converters

There is an 11-channel analog-to-digital converter in UEM. The AD converters are calibrated in the production line.

BB-RF Interface Connections

All the signal descriptions and properties in the following tables are valid only for active signals.

Table 1: PDM Interface

Signal name	From	To	Parameter	Min	Typ	Max	Unit	Function
RX_IF_AGC	UPP GenIO 9	Batman	Voltage Min Max --- Clk Rate (1)	0.0 1.75 ---	1.8 --- 9.6	0.1 1.86 --- 19.2	V --- MHz	Controls gain of VGA r in receiver
TX_IF_AGC	UPP GenIO 7	Robin	Voltage Min Max --- Clk Rate (1)	0.0 1.75 ---	1.8 --- 9.6	0.1 1.86 --- 19.2	V --- MHz	Controls gain of VGA in IF VGA in Robin
TX_RF_AGC	UPP GenIO 26	Robin	Voltage Min Max --- Clk Rate (3)	0.0 1.75 ---	1.8 --- 9.6	0.1 1.86 --- 19.2	V --- MHz	Controls gain of TX driver in Robin
PA_GAIN	UPP GenIO 19	Robin	Voltage Min Max --- Clk Rate (3)	0.0 1.75 ---	1.8 --- 9.6	0.1 1.86 --- 19.2	V --- MHz	Controls gain of PA

Table 2: General I/O Interface

Signal name	From	To	Parameter	Input characteristics	Function
TX_Gate	UPP Gen IO 8 pullup	Robin	"1" Transmitter Off "0" Transmitter On Timing Accuracy	1.38 1.88 V 0 0.4 V 4 chips, and can be up to a total of 255 chips	Punctures the PA's and the Robin ASIC Digital Into RF
PA_Boost	UPP Gen IO 28 pullup	Snapper Shark	"1" boost mode "0" data mode Timing Accuracy	1.38 1.88 V 0 0.4 V 4 chips, and can be up to a total of 255 chips	Sets PA current for desired linearity Digital Into RF

Table 3: VCTCXO Interface

Signal name	From	To	Parameter	Min	Typ	Max	Unit	Function
CLK192M_UPP	VCTCXO	Upp Batman Robin UHF PLL	Frequency --- Signal amplitude	--- 0.5	19.2 --- 1.0	--- 1.5	MHz --- Vpp	High stability clock signal for logic circuits, AC coupled sinewave. Analog Out of RF
AFC	UEM	VCTCXO	Voltage Min Max --- Settling time (4)	0.0 2.4 ---	---	0.1 2.55 --- 0.2	V --- ms	Automatic frequency control signal for VCTCXO Digital Into RF

Table 4: Regulated Supplies from UEM to RF

Signal name	From	To	Parameter	Min	Typ	Max	Unit	Function
VBAT	Battery	PA & UEM, external driver amps	Voltage --- Current	3.2 --- 0	3.5 ---	5.1 --- 2A peak	V ---	Battery supply. Lower limit is to guarantee regulator PSRR
VR1A	UEM	UHF Synth	Voltage --- Current	4.6 --- 0	4.75 --- 4	4.9 --- 5	V --- mA	Charge pump + linear regulator.
VR1B	UEM	PA Iref current sources in Robin	Voltage --- Current	4.6 --- 0	4.75 --- 4	4.9 --- 5	V --- mA	Charge pump + linear regulator
VR2	UEM	Robin driver amps	Voltage --- Current	2.70 ---	2.78 ---	2.86 --- 100	V --- mA	Linear regulator
VR3	UEM	VCTCXO Robin VHF synthesizer	Voltage --- Current	2.70 ---	2.78 ---	2.8 --- 20	V --- mA	Low noise linear regulator for VCTCXO
VR4	UEM	UHF VCO, synthesizer	Voltage --- Current	2.70 ---	2.78 ---		V --- mA	Low Iq linear regulator
VR5	UEM	Batman IF, BB, LNA, mixer	Voltage --- Current	2.70 ---	2.78 ---		V --- mA	Low Iq linear regulator
VR6	UEM	Robin IF, BB, mixers	Voltage --- Current	2.70 ---	2.78 ---		V --- mA	Low Iq linear regulator
VR7	UEM	Batman VHF synthesizer	Voltage --- Current	2.70 ---	2.78 ---		V --- mA	Low noise linear regulator for synthesizer
VREFRF01	UEM	Batman Vref	Voltage	1.334	1.35	1.366	V	Voltage Reference for RF-IC 1.2% accuracy

Table 4: Regulated Supplies from UEM to RF

Signal name	From	To	Parameter	Min	Typ	Max	Unit	Function
VREFRF02	UEM	Robin Vref	Voltage	1.334	1.35	1.366	V	Voltage Reference for RF-IC 1.2% accuracy
VIO	UEM	Digital IO + PLL digital	Voltage ---------- Current	1.70 ------	1.8	1.88 ------ 50	V ------ mA	Supply for RF-BB digital interface and some digital parts of RF.

Table 5: Slow A/D Converters

Signal name	From	To	Parameter	Min	Typ	Max	Unit	Function
PA_TEMP	Thermistor	UEM	Input voltage range ---------- Input clock freq	0 -------	 ------	2.741 -------- 2.5	V ------ MHz	PA temperature sensor output voltage Analog Out of RF
PWROUT	Robin	UEM	Input voltage range ---------- Input clock freq	0 -------	 ------	2.741 -------- 2.5	V ------ MHz	Buffered output of TX output detector and TX power supply Analog Out of RF
FALSE_DET	Robin	UEM	Input voltage range ---------- Input clock freq	0 -------	 ------	2.741 -------- 2.5	V ------ MHz	protection circuit that is independent of main transmitter on-off control circuit and minimizes the possibility of false transmission caused by component failure

Table 6: RF-BB Analog Signals

Signal name	From	To	Parameter	Min	Typ	Max	Unit	Function
RX_IP_RF RX_IN_RF RX_QP_RF RX_QN_RF	Batman	UEM	Differential voltage swing (static) ---------- DC level ---------- Input Bandwidth	1.35 -------- 1.3 --------	1.4 ------- 1.35 -------	1.45 -------- 1.4 -------- 615	Vpp ------- V ------- kHz	Differential in-phase and quadrature RX baseband signal Analog Out of RF
TX_IP_RF TX_IN_RF TX_QP_RF TX_QN_RF	UEM	Robin	Differential voltage swing (static) ---------- DC level ---------- -3 dB Bandwidth	 -------- 1.65 -------- 650	0.9 ------- 1.7 -------	1.0 ------- 1.75 -------- 1950	Vpp ------- V ------- kHz	Differential quadrature phase TX baseband signal for RF modulator Analog into RF

Table 7: RFIC Control

Signal name	From	To	Parameter	Min	Typ	Max	Unit	Function
RF_BUS_CLK RF_BUS_DATA RF_BUS_EN1X	UPP	Robin/Batman/ PLL	High-level input voltage, V_{IH} Low-level input voltage, V_{IL} High-level output voltage, V_{OH} Low-level output voltage, V_{OL} Clock	1.2 1.3	1.3 1.4 9.72	2.35 0.5 2.45 0.4	V V V V MHz	Serial Clock = Digital Into RF Bidirectional Serial Date = Digital I/O Latch enable for Batman and Robin = Digital Into RF
SYNTH_LE	UPP	PLL	Voltage Timing resolution	0		1.8 10	V us	Synthesizer latch enable

Table 8: RFIC Control

Signal name	From	To	Parameter	Min	Typ	Max	Unit	Function
PURX	UEM	Robin/Batman	Voltage Level ---------- Timing resolution	0 --------	-------	1.8 -------- 10	V ------ us	Power Up Reset for Batman and Robin

UPP

UPP Introduction

NPD-4 uses UPP8Mv2.2 ASIC. The RAM size is 8Mbit. The UPP ASIC is designed to operate in a DCT4 engine, and is designed as part of the DCT4 common baseband task force. The DCT4 processor architecture consists of both DSP and MCU processors.

Blocks

UPP is internally partitioned into two main parts: the Brain and the Body.

The Brain consists of the Processor and Memory System (*i.e.,* Processor cores, Mega-cells, internal memories, peripherals, and external memory interface). The following blocks are included: the DSP Subsystem (DSPSS), the MCU Subsystem (MCUSS), the emulation control EMUCtl, the program/data RAM PDRAM, and the Brain Peripherals–subsystem (BrainPer).

The Body consists of the NMP custom cellular logic functions. These contain all interfaces and functions needed for interfacing with other DCT4 baseband and RF parts. It includes the following sub-blocks: MFI, SCU, CTSI, RxModem, AccIF, UIF, Coder, GPRSCip, BodyIF, SIMIF, PUP, and CDMA (Corona).

Flash Memory

Introduction

Flash memory is a high-performance, 64-Mbit, single power supply 1.8 Volt-only FLASH memory device. This device is designed to be programmed in-system with the standard system 1.8-volt Vcc supply. A 12.0 volt Vpp is not required for program or erase operations, although an acceleration pin is available if faster write performance is required. The device is a boot-sectored device, consisting of eight 8Kb and 63 sectors of 64Kb each.

The device has two read modes: asynchronous read and burst mode read. Device powers-up in an asynchronous read mode. In the asynchronous mode, the device has two control functions which must be satisfied in order to obtain data at the outputs. In the linear mode, the device will deliver a continuous sequential word stream starting at the specified word and continuing until the end of the memory or until the user loads in a new starting address or stops the burst advance. The burst mode read operation is a synchronous operation tied to the rising edge of the clock. The microprocessor supplies only the initial address; all subsequent addresses are automatically generated by the device at the rising edge of subsequent clock cycles. The burst read cycle consists of an address phase and a corresponding data phase. The device also is capable of Burst Suspend and Burst Resume operations.

In order to reduce the power consumption on the bus, a Power Save function is introduced. This reduces the amount of switching on the external bus.

User Interface Hardware

LCD

Introduction

The 3585i uses a 96x65 grayscale display. Dimensions for display are 38.4mm x 37.6mm x 1.7mm with an active area of 30.6 mm x 24.1mm. The display supports six lines of graphics or text using Jack 3.4 UI style.

Interface

LCD is controlled by UI SW and control signals.

Booster capacitor (C303 100nF) is connected between booster pin (Vout) and ground. The capacitor stores boosting voltage.

Keyboard

Introduction

NPD-4 keyboard design is Nokia Jack style, with up and down navigation keys, two soft keys, 12 number keys, and side volume keys. The PWR key is located on top.

Power Key

All signals for keyboard are coming from UPP asic except pwr key signal which is connected directly to UEM. Pressing of pwr key is detected so that switch of pwr key connects PWONX is of UEM to GND and creates an interrupt.

Keys

Other keys are detected so that when a key is pressed down, the metal dome connects one S-line and one R-line of UPP to GND and creates an interrupt for SW. Matrix of how lines are connected and which lines are used for different keys is described in the following table. S-line S0 and R-line R5 are not used.

Returns / Scans	S1	S2	S3	S4
R0	NC	Send	End	NC
R1	Soft left	Up	Down	Soft right
R2	1	4	7	*
R3	2	5	8	0
R4	3	6	9	#

NC = Not Connected

Lights

Introduction

NPD-4 has six white LEDs for lighting purposes: two (V309-V310) are for keyboard (type CL-270WB-D) and four (V303-V306) are for display (type CL-191WB-D). LED type is white-light emitting diode.

Interfaces

Display lighting and keyboard lights are controlled by UEM Klight signal (8-bit register DriverPWMR, bits 7...4). Klight output is Pulse Width Modulation (PWM) signal, which is used to control average current going through LEDs. A constant current source is used to ensure that the LEDs provide uniform intensity and color.

Technical Information

LEDs have white plastic body around the diode itself, which directs the emitted light to UI side. Current for keypad lights is limited by resistor between Vbatt and LEDs.

Vibra

Introduction

Vibra is located on the D-cover and is connected by spring connectors on the PWB. It is located in the left bottom side of the engine.

Interfaces

Vibra is controlled by pwm signal VIBRA from UEM. This signal allows control of both frequency and pulse width of signal. Pulse width is used to control current when battery voltage changes. Frequency control searches for optimum frequency to ensure silent and efficient vibrating.

Parameter	Requirement	Unit
Rated DC Voltage	1.3	V
Rated speed	9500 ±3000	rpm
Rated current	115 ±20	mA
Starting current	150 ±20	mA
Armature resistant	8.6	ohm
Rated DC voltage available	1.2 to 1.7	V
Starting DC voltage	min. 1.2	V

Audio Hardware

Earpiece

Introduction

The 13 mm speaker capsule that is used in DCT3 products also is used in NPD-4. The speaker is dynamical—very sensitive, and capable of producing relatively high sound pressure at low frequencies. The speaker capsule and surrounding mechanics comprise the earpiece.

Microphone

Introduction

The microphone is an electric microphone with omnidirectional polar pattern. It consists of an electrically polarized membrane and a metal electrode, which form a capacitor. Air pressure changes (*i.e.,* sound) move the membrane, which causes voltage changes across the capacitor. Since the capacitance is typically 2 pF, a FET buffer is needed inside the microphone capsule for the signal generated by the capacitor. The microphone needs bias voltage as a result of the FET.

MIDI Speaker

Introduction

Musical Instrument Digital Interface (MIDI) defines the data interchange format. By implementing MIDI engine in Expedition, enriched sound effect will be achieved, which includes: ringing tones, UI event sounds, and music for games and entertainment.

The MIDI data stream is a unidirectional, asynchronous bit stream at maximum

31.25 kbits/sec. with 10 bits transmitted per byte (a start bit, 8 data bits, and one stop bit).

MIDI data includes two categories of signals: MIDI tones and Alerting Tones. Both are generated from DSP and send to the MIDI speaker.

Audio Amplifier Interface

From audio hardware point, since the audio output from UEM is not strong enough to produce enough power for the speaker, an audio amplifier is required.

The MIDI audio signal generated by the DSP and UEM audio CoDec is routed to the XEAR output of the UEM. An audio amplifier is used to boost enough power for the speaker. GENIO (28) is used to enable/disable the audio amplifier as needed. Figure 2 is a block diagram of the audio hardware section for MIDI.

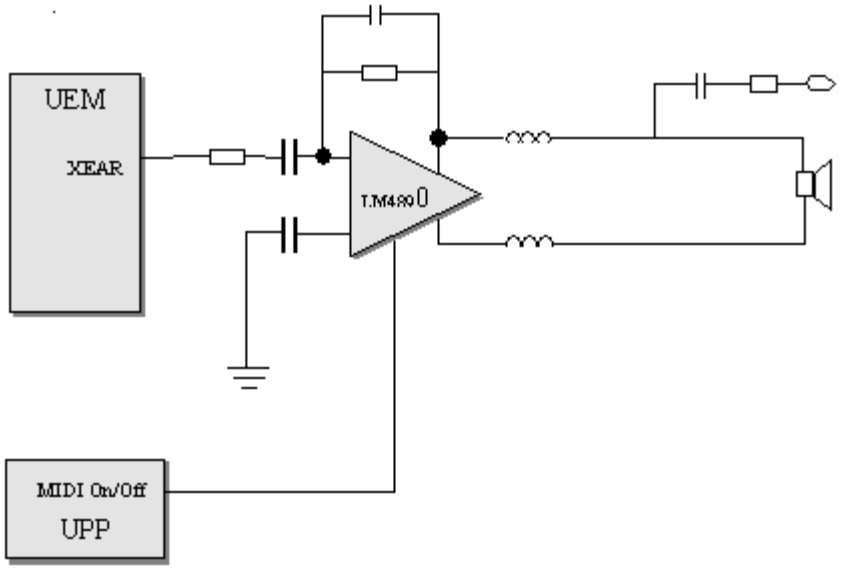


Figure 2: Audio HW section for MIDI

Battery

Phone Battery

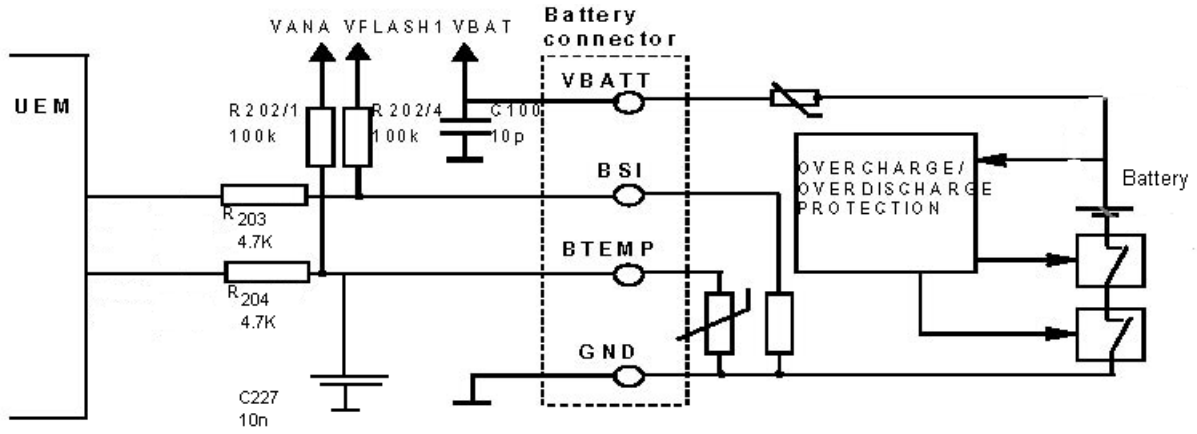
Introduction

A 950 mAh Li-ion battery (BLC-2) is standard in NPD-4.

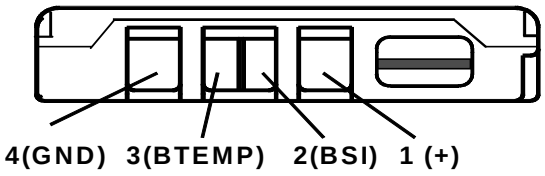
Interface

The battery block contains NTC and BSI resistors for temperature measurement and battery identification. The BSI fixed resistor value indicates the chemistry and default capacity of a battery. NTC resistor measures the battery temperature. Temperature and capacity information is needed for charge control. These resistors are connected to the BSI and BTEMP pins of battery connector. Phone has pull-up resistors (R202) for these lines so that they can be read by A/D inputs in the phone (see the following figure).

Resistor array (R206) is ESD protection. There also are spark caps in the BSI and BTEMP lines to prevent ESD.



Batteries have a specific red line to indicate if the battery has been subjected to excess humidity. The batteries are delivered in a "protection" mode, which gives longer storage time. The voltage seen in the outer terminals is zero (or floating), and the battery is activated by connecting the charger. Battery has internal protection for overvoltage and overcurrent.



Battery Connector

NPD-4 uses a spring-type battery connector. This makes the phone easier to assemble in production and ensures a more reliable connection between the battery and PWB.

#	Signal name	Connected from - to	Batt. I/O	Signal properties A/D--levels--freq./timing	Description / Notes
1	VBAT	(+) (batt.)	VBAT	I/O	Vbat
2	BSI	BSI (batt.)	UEM	Out	Ana.
3	BTEMP	BTEMP (batt.)	UEM	Out	Ana.
4	GND	GND	GND		Gnd

Accessories Interface

System connector

Introduction

NPD-4 uses the Tomahawk accessories via the Tomahawk connector.

Interface

Tomahawk bottom connector consists of charging plug socket and Tomahawk System connector (see figures that follow). Minimum configuration of Tomahawk interface includes charging, mono audio, power out, ACI and Fbus. USB and stereo audio out are optional.

Tomahawk system connector includes:

- Charging

  Pads for 2 -wire charging in cradles

- Audio (Stereo audio optional)

  4 -wire fully differential stereo audio

  FM radio antenna connection

  2-wire differential mic input

- Power out

  2.78V 70 mA output to accessories (bb4.0, bb4.5)

  2.5V 90 mA output to accessories (bb5.0)

- Detection/controlling

  ACI

  Point to point bi-directional data line

- USB (Optional)

  Power in 5V in from USB host

  USB v2.0 device mode (Full speed 12M)

- Fbus

Standard Fbus

AT command mode (Nokia Serial Bus)

Phonet message mode

Fast Fbus, fast data bus to add on modules

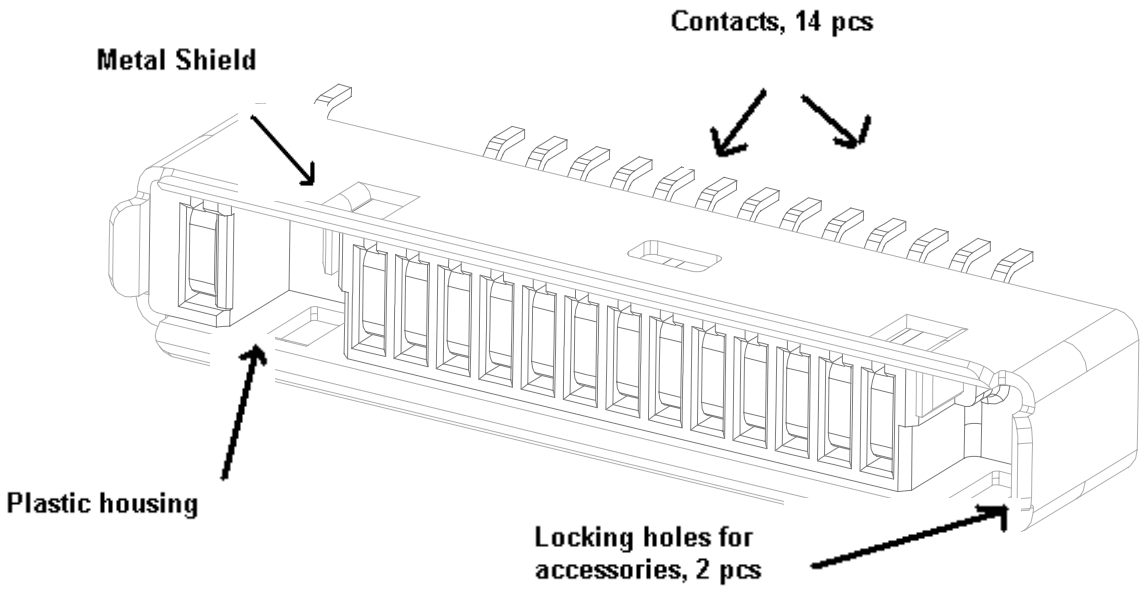


Figure 3: Tomahawk system connector

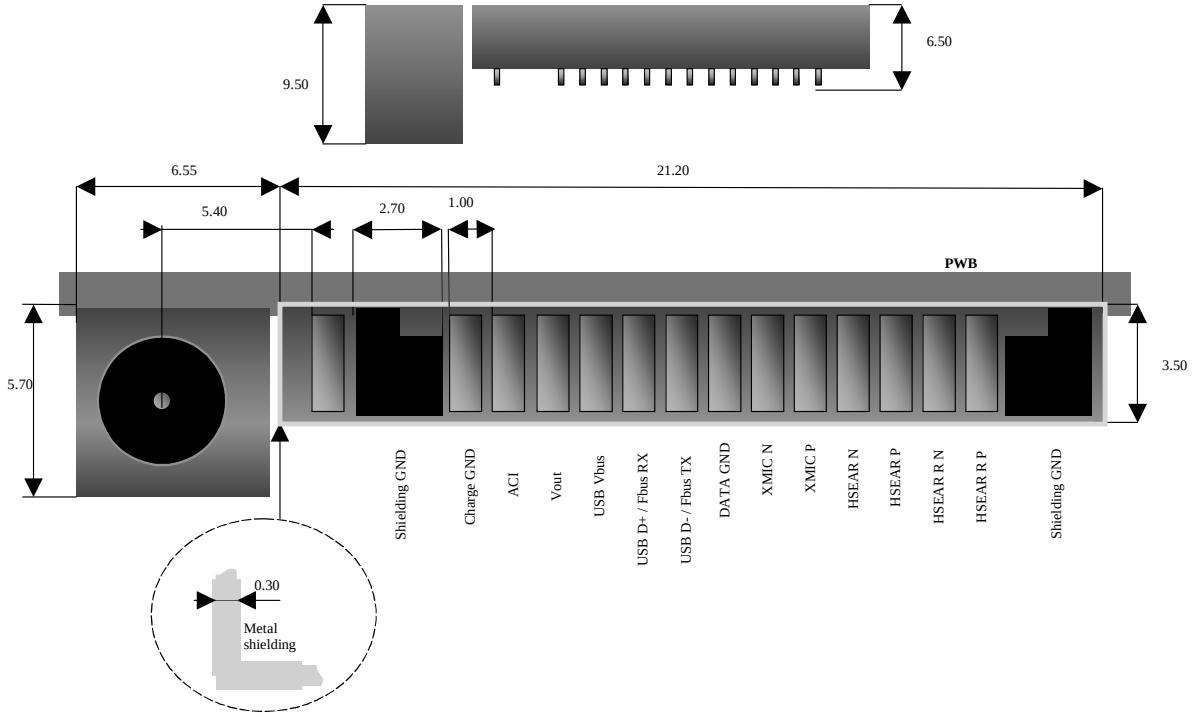


Figure 4: Mechanical dimensions and signals of Tomahawk bottom connectors

An accessory is detected by the ACI-line. All accessories will generate interrupt while inserted or removed from the phones Tomahawk system connector. Insertion of an accessory will generate HEADINT interrupt by pulling ACI line down. Vout is enabled by UPP. The MBUS line is connected to HEADINT line. If HEADINT interrupt from low to high transition occurs within 20msec a more advanced accessory is connected else a basic headset is connected. The accessory flowchart outlines the routines used for all accessory detection.

The following diagram illustrates accessory detection / external audio flowchart.

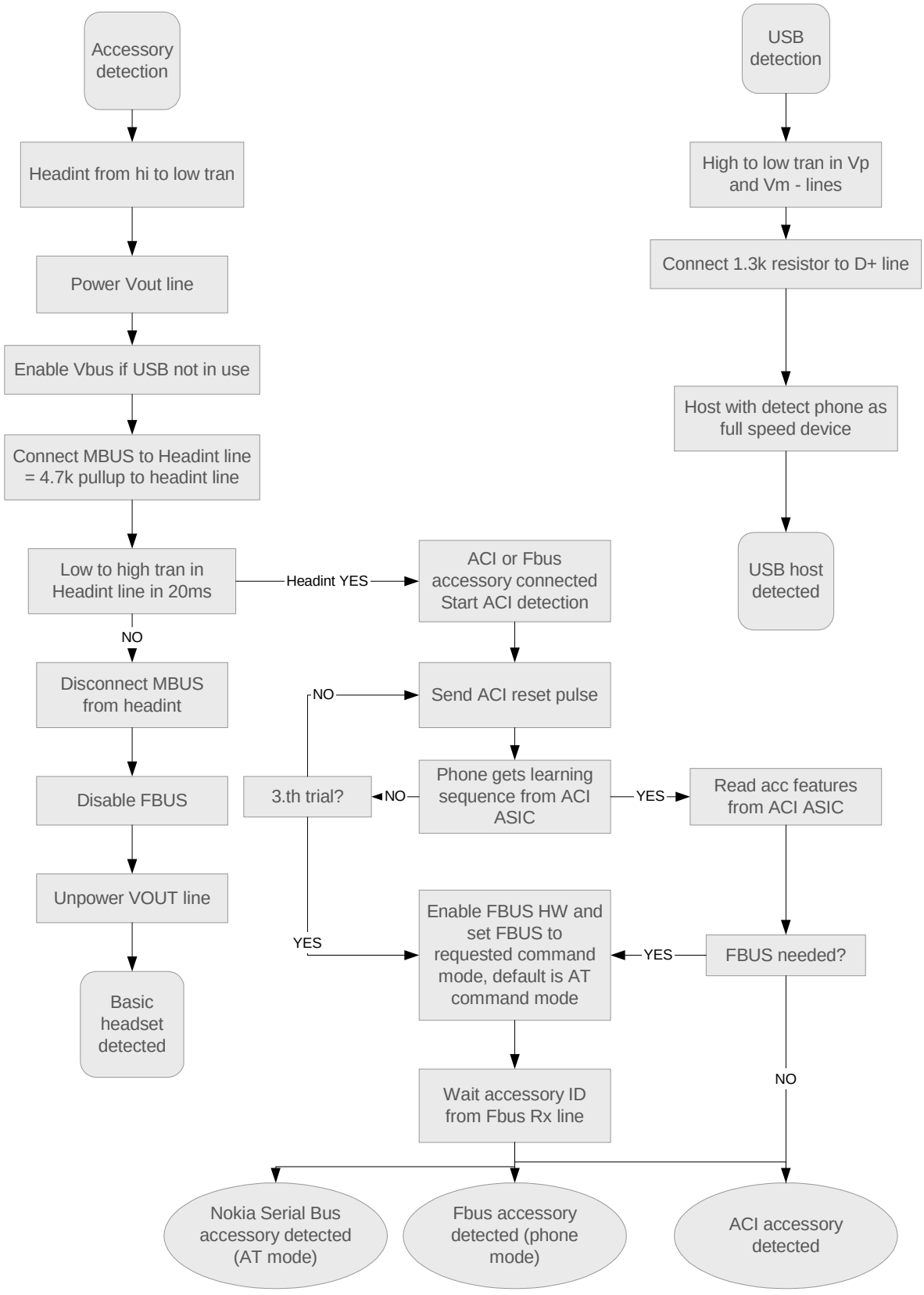


Figure 5: Accessories Detection Flowchart

TTY/TTD and Universal Headset Jack

TTY/TDD devices use standard 2.5mm 3-pin plug (tip = transmit, ring = receive, sleeve = ground) while universal headset also use same type of plug (tip = microphone, ring = earpiece, sleeve = ground). Since only three pins are available for both transmit and receive at same time, both paths have to use single-end design (share the ground). The detection scheme for this interface uses a built-in normally closed switch in the universal headset jack. When there is no device being plugged in, the switch is closed which forces the level on the detection line (GENIO(12)) to 1.8V. When a device is plugged in, the voltage is set to 0V. The detection line then can identify whether a device is plugged in or not.

Charger IF

Introduction

The charger connection is implemented through the bottom connector. DCT-4 bottom connector supports charging with both plug chargers and desktop stand chargers.

There are three signals for charging. Charger gnd pin is used for both desktop and for plug chargers as well as charger voltage. PWM control line, which is needed for 3-wire chargers, is connected directly to gnd in module PWB so the NPD-4 engine doesn't provide any PWM control to chargers. Charging controlling is done inside UEM by switching UEM internal charger switch on/off.

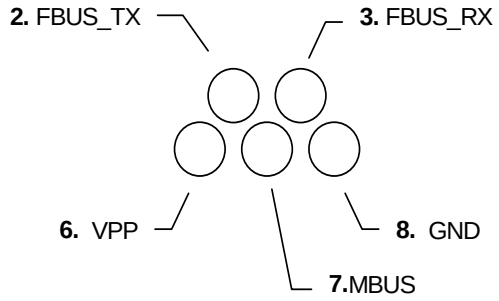
Interface

The fuse F100 protects from high currents (e.g. ,when broken or pirate chargers are used). L100 protects engine from RF noises that may occur in charging cable. V100 protects UEM ASIC from reverse polarity charging and from high charging voltage. C106 is also used for ESD and EMC protection.

Test Interfaces

Production Test Pattern

Interface for NPD-4 production testing is 5-pin pad layout in BB area (see figure below). Production tester connects to these pads by using spring connectors. Interface includes MBUS, USRX, FBUSTX, VPP, and GND signals. Pad size is 1.7mm. The same pads also are used for AS test equipment such as module jig and service cable.



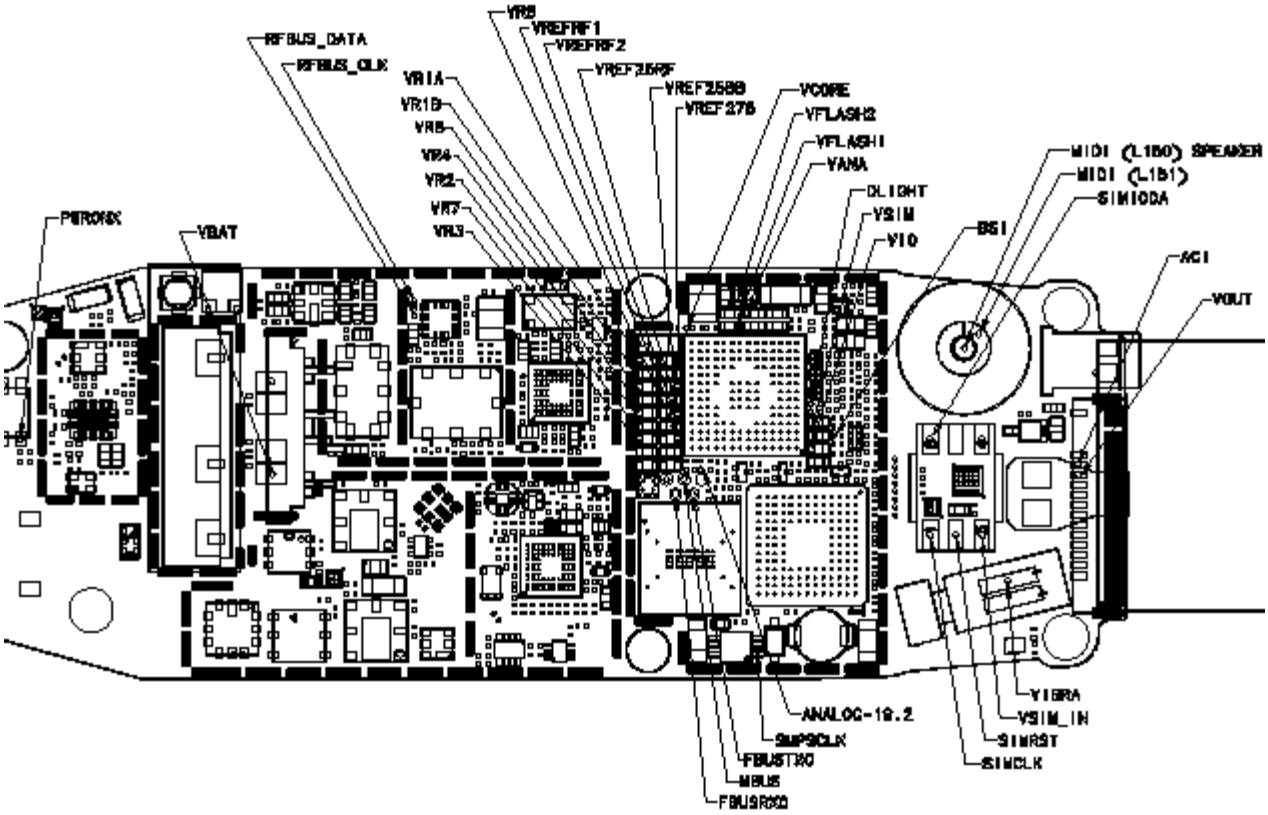


Figure 6: 3585i Test Points - Top

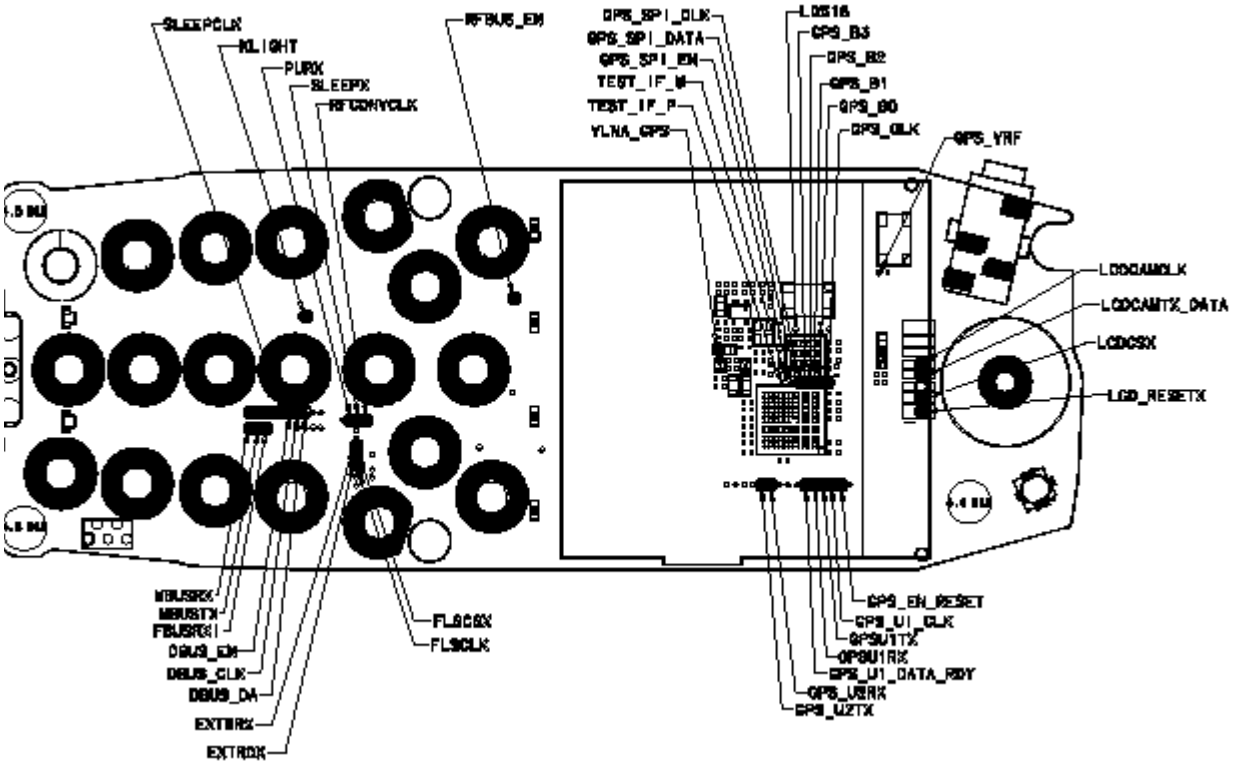


Figure 7: 3585i Test Points - Bottom

EMC

General

EMC performance of the NPD-4 baseband is improved by using a shield to cover main components of BB, such as UEM, UPP, and Flash. UEM has internal protection against ±8kV ESD pulse. BB shield is soldered into PWB and it also increases the rigidity of PWB in BB area, thus improving phone reliability. Shield also improves thermal dissipation by spreading the heat more widely.

A protective metal deck is located underneath the battery and is grounded to both the BB shield and the RF shield.

BB Component and Control I/O Line Protection

Keyboard Lines

ESD protection for the keyboard is provided by component Z300. This device is designed to reduce EMI and RFI noise. In addition, this intergrated device includes ESD protection circuitry that will protect the phones ASICs from destruction when subjected to ESD surges up to 15kV.

PWB

All edges are grounded from both sides of PWB and solder mask is opened from these areas. Target is that any ESD pulse faces ground area when entering the phone (e.g., between mechanics covers). All holes in PWB are grounded and plated through holes.

Tomahawk Lines

FBUS and ACI lines are protected by V101.

General Information About Testing

Phone operating modes

Phone has three different modes for testing/repairing phone. Modes can be selected with suitable resistors connected to BSI- and BTEMP- lines as follows:

Mode	BSI- resistor	BTEMP- resistor	Remarks
Normal	68k	47k	
Local	560_ (<1k_)	What ever	
Test	> 1k	560_ (<1k_)	Recommended with baseband testing. Same as local mode, but making a phone call is possible.

The MCU software enters automatically to local or test mode at start-up if corresponding resistors are connected.

Note! Baseband doesn't wake up automatically when the battery voltage is connected (normal mode).

Power can be switched on by

- pressing the PWR key
- connecting a charger
- RC-alarm function

In the local and test mode, the baseband can be controlled through MBUS or FBUS (FBUS is recommended) connections by Phoenix service software.

RF Module

Requirements

The NPD-4 RF module supports CDMA1900 and CDMA 800 as described in:

• IS2000-2-A Physical Layer Standard for cdma2000 Spread Spectrum Systems; and

• IS-98D (Draft 4) Recommended Minimum Performance Standard for Spread Spectrum Mobile Stations.

Temperature Conditions

Surface temperature (SPR5 - Product Safety)

Maximum temperature rise is 50^{o} C for nonmetallic surfaces and 30^{o} C for metal surfaces at room temperature.

Other temperature requirements (SPR4 - Operating Conditions)

Meeting requirements: -30...+ 60^{o} C

Storage requirements: -30...+85^{o} C

Main Technical Characteristics

Environmental Specifications

Normal and extreme voltages

Voltage range:

- nominal battery voltage: 3.6 V
- maximum battery voltage: 4.5 V
- minimum battery voltage: 3.2 V

Temperature conditions:

- ambient temperature: -30...+ 60^{o} C
- PWB temperature: -30...+85^{o} C
- storage temperature range: -40 to +85^{o} C

Antenna

A dual-band, whip antenna/internal antenna combination is used. The GPS antenna is an IFA type, embossed on top of the main antenna module.

Transmitter

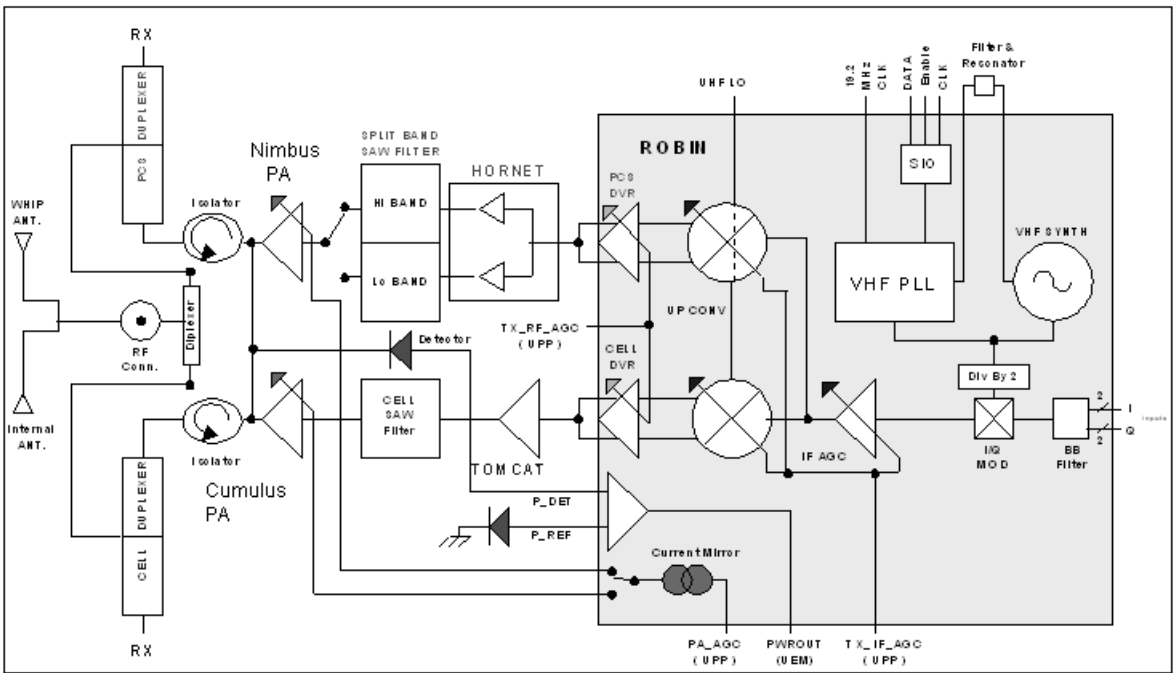


Figure 8: Trimode block diagram

The transmit chain up to the RF driver stage is integrated into one transmit-integrated

circuit called Robin, with external power amplifiers (PA). The channel spacing is 50 kHz.

All data transmitted on the channel is convolutionally encoded and block-interleaved. Modulation is 64-ary orthogonal (RC1 and RC2) and direct sequence spread by a quadrature pair of PN sequences at a fixed chip rate. The data is filtered, O-QPSK modulated and up-converted to the appropriate transmission frequency. RC3 and RC4 use HPSK modulation at data rates up to 153.6 kBPS (RC3) and 115.2 kBPS (RC4).

The baseband I/Q signals are converted to IF frequency in the I/Q modulator by Quadrature mixing. The modulated IF signals go through a variable gain amplifier (IF AGC) and then are routed either to the PCS TX path or the Cell TX path. The path consists of an upconverter and a variable gain RF amplifier. The IF signal is converted up to RF with a differential output upconverter and then fed to the RF amplifier. The RF amplifier has variable gain capability (RF AGC) with up to 40 dB of dynamic gain control.

The outputs of the RF amplifiers are differential. The differential outputs from Robin are combined into single-ended output by an external balun and fed into an external driver amplifier module (Hornet for PCS and Tomcat for cell). There are two outputs from this module that feed a split-band filter. The split-band filter output is connected to a SPDT RF switch that results in a single output.

This split-band filter provides the needed Rx band rejection performance. The wide PCS Tx band (60 MHz) and small separation (20 MHz) between TX and Rx band prevents a single SAW filter from achieving the required Rx rejection. As a result, the PCS band SAW filter is divided into two bands, each 35 MHz wide.

The output of the SPDT RF switch then is connected to the PA (Nimbus). Out of the PA is an isolator, then antenna.

The PA modules contain all the necessary matching networks and reference current circuitry for variable gain control and biasing ON/OFF. A variable reference current is used to vary the PA gain and PA bias current. The variable gain technique reduces PA current consumption and improves the signal-to-noise ratio at low output power levels. The precision bias current (and gain) control is achieved by varying the PA reference current with a PDM control voltage.

The transmitter chain utilizes smart power techniques and only the required circuits are powered at the appropriate times. In order to save energy in puncture mode, when there is no speech activity during a call, the driver and power amplifiers and the Robin IC are switched ON and OFF rapidly. These units also are in the OFF state when the transmitter is in standby. The ON/OFF switch commands are issued by a Digital ASIC (UPP). The UPP's PDM controls a current mirror in Robin that provides the PA reference current. Switching each reference current ON/OFF switches each PA ON/OFF. The VHF synthesizer and power detector circuits are left on during the puncture mode.

Synthesizer

Refer to Figure 7 for a block diagram that illustrates all three synthesizers and how they interconnect in the system.

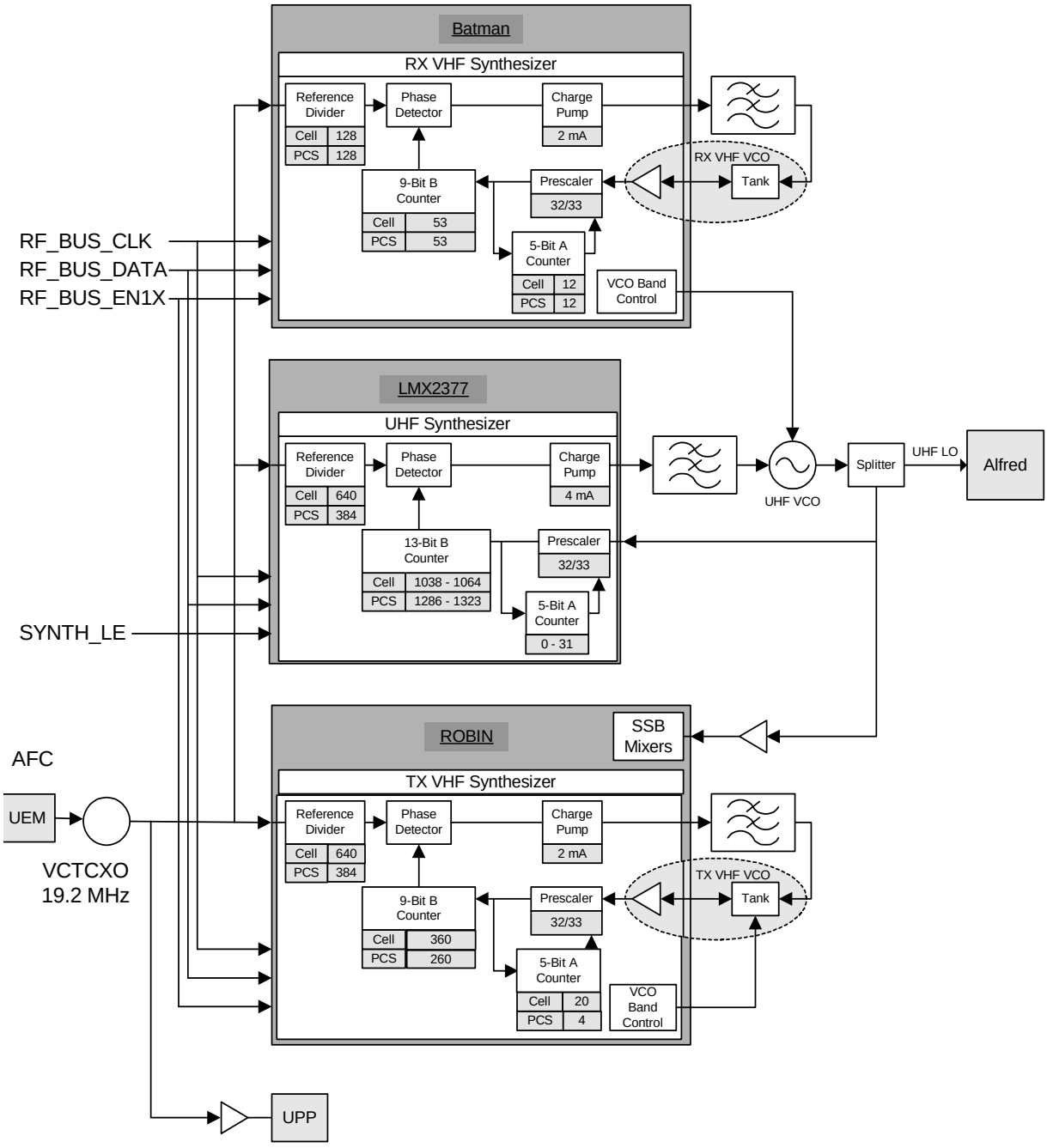


Figure 9: Synthesizer System Block Diagram

UHF LO Synthesizer

The UHF LO synthesizer generates the first RX LO frequency for the receiver (down-conversion) and the second TX LO frequency for the transmitter (up-conversion). The synthesizer is a dual-modulus prescaler type and utilizes a phase-frequency detector with a

charge pump that sinks or sources currents, depending upon the phase difference between the phase detector input signals.

For PCS, channel spacing and the comparison frequency is 50 kHz. For the cellular AMPS/ CDMA band, channel spacing is 50 kHz. An external buffer is provided for high isolation between Robin and the VCO to reduce VCO pulling due to changing load.

1st TX VHF LO Synthesizer (Robin)

The TX VHF Synthesizer is integrated within the Robin RFIC and generates the LO signals for the IQ-modulator in Robin. The synthesizer has an internal VCO with an external resonator. The VCO operates at two times the CELL and PCS IF frequencies. A band-switch signal, VCO_Band, is used to shift the center frequency of the external resonator.

The synthesizer is a dual-modulus prescaler type, and utilizes a phase detector with a charge pump that sinks or sources currents, depending on the phase difference between the detector input signals. The width of the pulses depends on the phase difference between the signals at input of the phase detector. The main divider, auxiliary divider, and reference divider are programmable through the serial interface to Robin.

The TX VHF Synthesizer generates 346.2 MHz for Cell Band and 416.2 MHz for PCS band.

The TX VHF Synthesizer comparison frequency for Cell Band is 50 kHz and PCS band is 50 kHz.

2nd RX VHF LO Synthesizer (Batman)

The RX VHF Synthesizer is integrated within the Batman RFIC and generates the LO signals for the IQ demodulator in Batman. The synthesizer has an internal VCO with an external resonator. The VCO operates at two times the common 128.1 MHz RX IF frequency. A band-switch signal, Band_Sel, is used to select the band of operation for the UHF VCO.

The synthesizer is a dual-modulus prescaler type, and utilizes a phase detector with a charge pump that signals or sources currents, depending upon the phase difference between the detector input signals. The width of the pulses depends on the phase difference between the signals at input of the phase detector. The main divider, auxiliary divider, and reference divider are programmable through the serial interface to Batman.

The RX VHF Synthesizer generates 256.2 MHz for both Cell Band and the PCS Band.

The RX VHF Synthesizer comparison frequency for both Cell Band and PCS Band is 150 kHz.

VCTCXO - System Reference Oscillator

The VCTCXO provides the frequency reference for all the synthesizers. It is a voltage-controlled, temperature-compensated, 19.2MHz crystal oscillator that can be pulled over a small range of its output frequency. This allows for an AFC function to be implemented for any frequency accuracy requirements. This is done by DSP processing of received I/Q signals.

Closed loop AFC operation allows very close frequency tracking of the base station to be done in CDMA mode. This will enable the unit to track out aging effects and give the required center frequency accuracy in cellular and PCS bands.

The most practical way of clock distribution is driving all three chips (UHF PLL, Batman, and Robin) directly from the VCTCXO. A buffer is used to drive the UPP in order to isolate the UPP's digital noise from the VCTCXO, which prevents contamination of the 19.2 MHz reference onto the PLL chips of the system. Since the VCTCXO output is a sinewave, such clock distribution will not cause any clock signal integrity problems, even for relatively long traces (what might occur in case of a digital square waveform with fast transition times). The VCTCXO output is AC, coupled to Batman, Robin, UFH PLL, and the digital ASICs (see figure) to eliminate DC incompatibility between those pins.

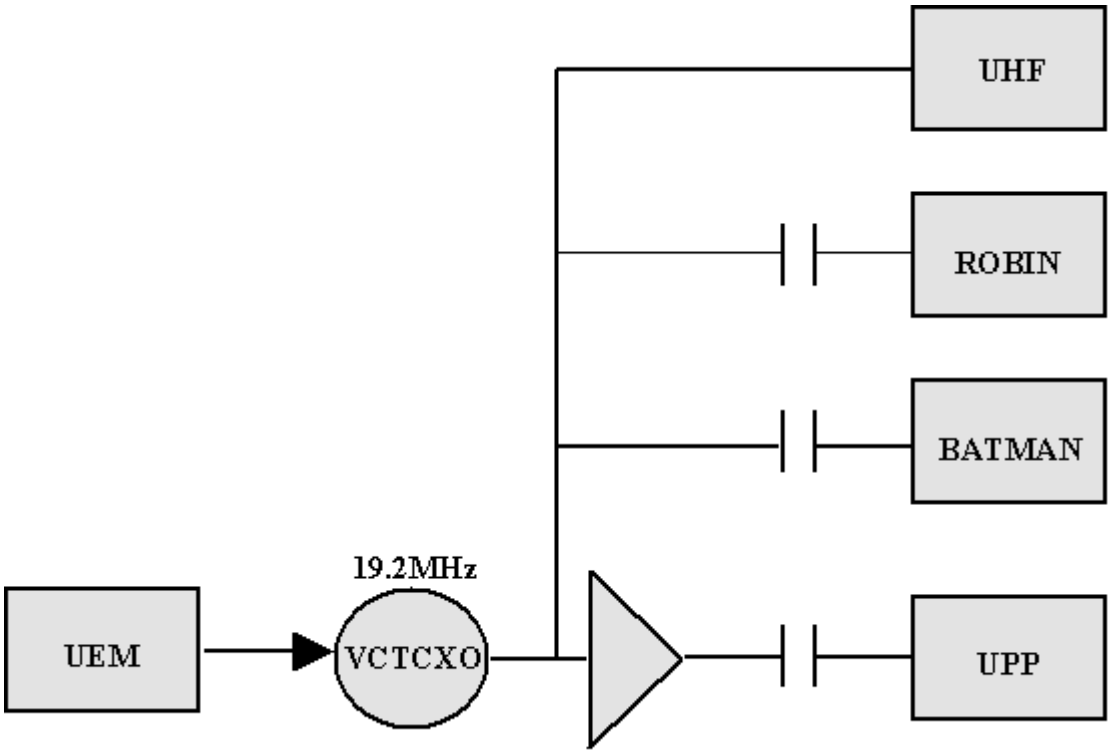


Figure 10: VCTCXO Clock Distribution

Receiver

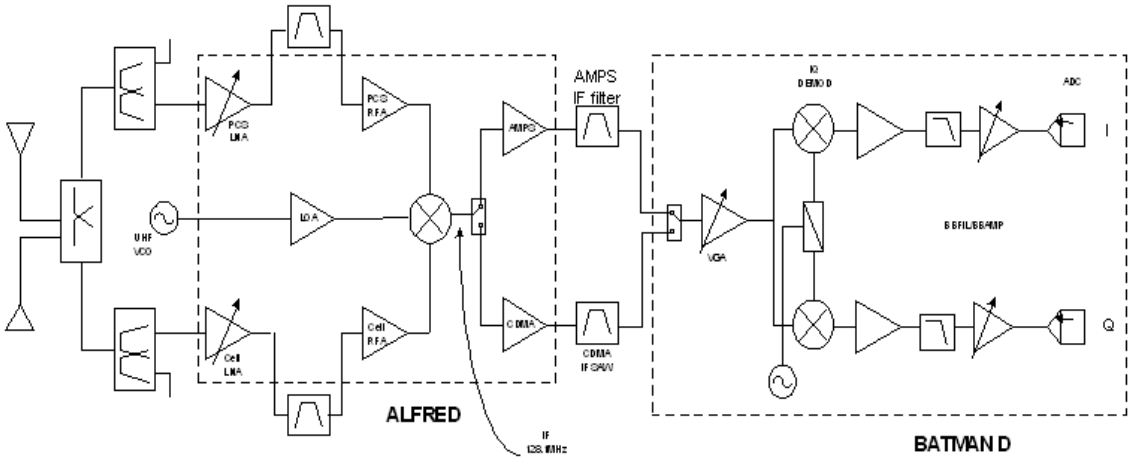


Figure 11: 3585i Receiver Block Diagram

The receiver is a dual conversion I/Q receiver with a first IF of 128.1 MHz. The front-end RFIC (Alfred) contains a low noise amplifier (LNA), a radio frequency amplifier (RFA), a down-converter, an intermediate frequency amplifier (IFA), and a local oscillator amplifier (LOA). Between the LNA and the RFA is a bandpass filter which will reject out-of-band spurious and act as image rejection. The IF filter is between the Alfred IC and the BatmanD IC. The purpose of this filter is to guarantee rejection in adjacent and alternate channels.

The RX IF ASIC BatmanD is used to convert the IF down to baseband I and Q. The ASIC contains a VGA section, IQ demodulator, baseband filters (BBFIL) for AMPS and CDMA. Switchable gain baseband amplifier (BBAMP), and RX VHF PLL. The I/Q BB signals are output to UEM chip for analog-to-digital conversion and further signal processing.

GPS Engine

Introduction

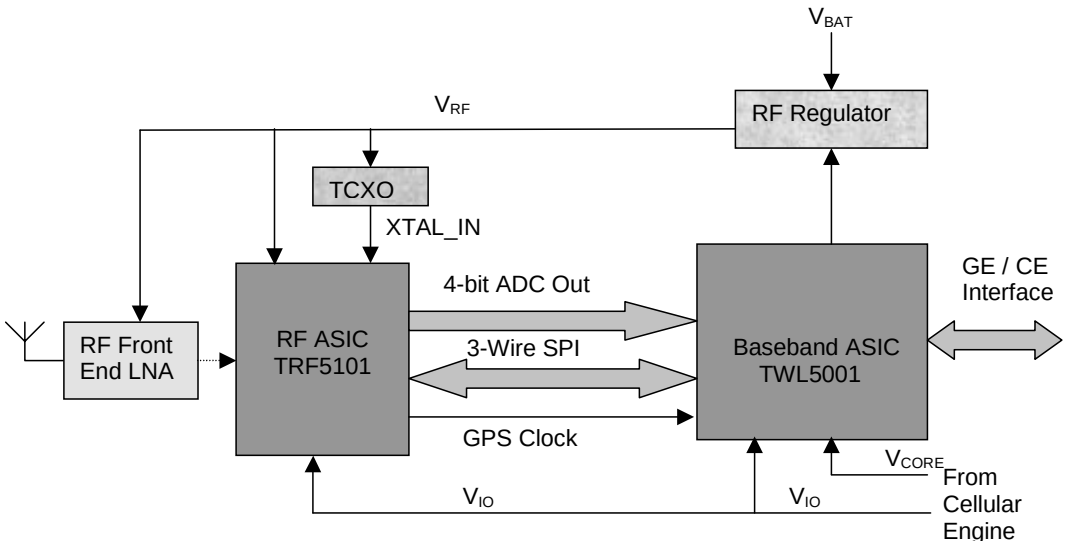


Figure 12: GPS Engine Block Diagram

The GPS engine (GE) major components consist of two ASICs, the RF Front End with a Low Noise Amplifier (LNA), a voltage regulator, and a Temperature-Controlled Crystal Oscillator (TCXO). The front end provides filtering of out-of-band signals and amplification of the frequency band of interest. The RF ASIC provides further amplification, AGC, down-conversion to low IF, IF filtering and analog to digital conversion of the IF. The baseband ASIC is responsible for all baseband processing of the GPS signal, including PN wipeoff, decoding, and GPS measurement calculations. The TCXO provides a 16.368 MHz signal for down-conversion and sampling and is used by the baseband ASIC for all the GPS processing. The RF regulator provides voltage regulation from the battery to provide 2.8 volts for the RF components.

The GE is controlled by the Cellular Engine (CE) via the GE/CE Interface. When the CE powers up, the GE performs a self-test and informs the CE of self-test results. If the self-test results pass, the CE will download the operational code to the GE via the GE/CE interface. If the self-test of the GE fails, the CE will declare a hardware failure and increment the "Test Mode 0 Failure" PPC. The CE will receive a GPS status message from the GE after download as to the success of the download. If the download fails, the CE will reset the GE, increment the "Code Download Failure" PPC, and try to download the code again. After the third unsuccessful attempt of download, the CE will declare a hardware failure and hold the GE in reset. If download is successful, it will configure the GE and then put the GE to sleep. Sleep is the normal state of the GE and the only time it is woken up is from any of the following:

- To perform periodic self-test
- When an IS-801.1 location session starts
- When a command is sent to it through the test interface in the Location Server SW in the CE, (e.g., a command from Phoenix)

During sleep of the GE, the RF regulator is off and the RF ASIC is powered down. The baseband ASIC remains powered on, but has no internal clocks running except the sleep clock from the CE.

GE / CE Interface

The GE / CE interface has various control signals, a reference clock, a sleep clock, and serial bus. There also are V_{CORE} and V_{IO} voltage generated in the CE baseband used to power some of the GE.

Digital Supply Vio

This supply is used to power the GPS RF/BB interface lines and also to preserve configuration settings in the RFIC when it is in power-down mode. It originates from the CE energy management system.

Parameter	Units	Min	Typ	Max
On Level	V	1.65	1.8	1.95
Load Current - Active	mA		1.6	3
Load Current – Sleep	µA		240	350

Digital Supply Vcore

This supply is used to power the internal GPS Baseband ASIC during operation and to preserve the internal state when it is in deep sleep mode. It originates from the CE energy management system.

Parameter	Units	Min	Typ	Max
On Level	V	1.425	1.5	1.65
Load Current - Active	mA		26	35
Load Current – Sleep	µA		30	500

Reference Clock (GPS_RFCLK)

The reference clock from the CE is 19.2 MHz sine wave from the VCTCXO in the CE. It is used by the GE to calibrate the GPS clock and for communication on the serial bus to/from the CE.

Parameter	Units	Min	Typ	Max
Frequency	MHz	-0.38 ppm	19.2 MHz	+0.38 ppm
Level	Volts p-p		1.0	

Sleep Clock (GPS_SLEEPCLK)

The sleep clock from the CE is 32 kHz square wave from the sleep clock generated in the CE. It is used by the GE to wake up from sleep and for a real-time clock function.

PA Enable (GPS_PA_EN)

The PA enable from the CE is high when the PA is on (transmitter is on). It is currently not used by the GE.

Reset (GPS_EN_RESET)

The reset signal is generated by the CE from a GenIO from UPP. When low, the GE is in a reset state and when high, the GE is enabled.

SleepX (GPS_SLEEPX)

The SleepX signal from the CE when transitioning from high to low, tells the GE that the CE is going to deep sleep. This means that the reference clock to the GE will be shut-down. Internal logic in the GPS baseband ASIC gates off the reference clock when SleepX goes low.

USART Receive (GPS_U1_RX)

The USART Receive signal is the serial communication from the CE to the GE. During normal operation, it is a low-voltage (1.8 volt) RS-232 protocol serial data receive signal operating at 57,600 bits per second. During code download, it operates as a high speed, synchronous receive data signal in conjunction with the USART clock and USART data ready signals. The data rate in this mode is 8.184 Mbps.

USART Transmit (GPS_U1_TX)

The USART Transmit signal is the serial communication from the GE to the CE. During normal operation, it is a low-voltage (1.8 volt) RS-232 protocol serial data transmit signal operating at 57,600 bits per second. During code download, it operates as a high-speed, synchronous transmit data signal in conjunction with the USART clock and USART data ready signals. The data rate in this mode is 8.184 Mbps.

USART Data Ready (GPS_U1_DATA_RDY-TIMESTAMP)

The USART Data Ready signal is a dual-purpose signal. During synchronous code download, the signal from the CE to the GE indicates that the CE has a byte to transmit on the USART Transmit data signal. To find a GPS signal in normal operation, when the GE is active, the CE sends a pulse once per second to the GE, indicating the exact time of CDMA. This is used by the GE to find the GPS signal much faster than normal.

USART Clock (GPS_U1_INT_CLK)

The USART Clock signal is a dual-purpose signal. During synchronous code download, the signal from the GE to the CE is the synchronous clock used by the CE to transmit/receive a byte on the USART TX/RX data lines. In normal operation, the GE can send a pulse on this signal to interrupt the CE, indicating an error or status change.

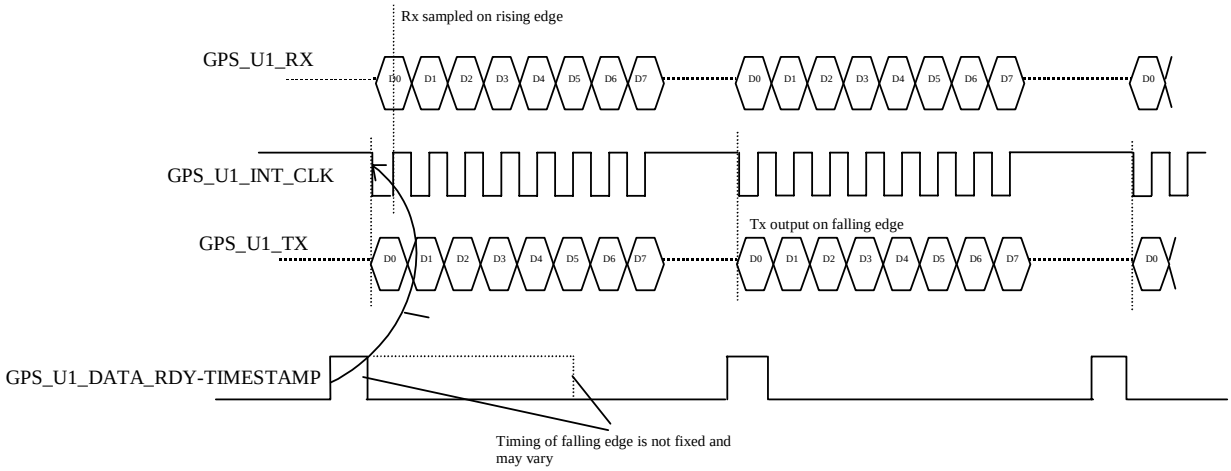


Figure 13: USART Signals During Synchronous Download

Digital GE/CE Interface Signal Parameters

Parameter	Units	Min	Typ	Max
Hi Level	Volts	0.8*Vio		
Lo Level	Volts			0.22*Vio

GPS RF Interface

This interface is between the GPS RF ASIC and GPS BB ASIC or the system.

RF ASIC and LNA Supply V_{RF}

The V_{RF} supply is the main source of power for the RF IC. It originates in GPS baseband section and will be turned off for power-saving sleep modes.

Parameter	Units	Min	Typ	Max
On Level	V	2.7	2.8	3.3
Load Current - Active	mA		40	55

GPS Clock

The GPS clock is an GPS RF to GPS baseband signal signal generated by the TCXO. It is used as a reference for the LO internal to the RF IC and is also fed out to the baseband IC as a reference clock for GPS timing.

Parameter	Units	Min.	Typ	Max
Frequency	MHz	-15 ppm	16.368	+15 ppm
Hi Level	Volts	0.8*Vio		
Lo Level	Volts			0.22*Vio
Duty Cycle	%	40		60

GPS ADC

The ADC in the GPS RF ASIC provides up to 4 bits of sampled data of the received GPS signal to the GPS baseband ASIC. It is clocked by the GPS clock.

Parameter	Units	Min.	Typ	Max
Bit Rate	bit/s	-15 ppm	16.368	+15 ppm
No. of Bits				4
Hi Level	Volts	0.8*Vio		
Lo Level	Volts			0.22*Vio

SPI Interface

The SPI interface between the GPS RF ASIC and the GPS Baseband ASIC consists of three signals : spi_clk, spi_en, and spi_data.

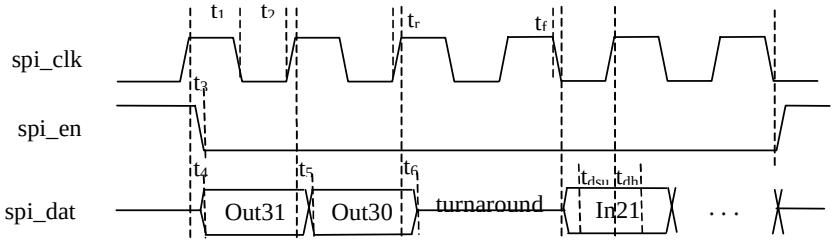


Figure 14: SPI Interface Example Relationship Diagram

SPI Clock (GPS_SPI_CLK)

The SPI clock is used to clock data to/from the GPS RF ASIC from/to the GPS Baseband ASIC. It is generated by the GPS Bandband ASIC to the GPS RF ASIC and is only active during data transfer.

Parameter	Units	Min	Typ	Max
Frequency	MHz		GPS Clock	
Hi Level	Volts	0.8*Vio		
Lo Level	Volts			0.22*Vio
Duty Cycle	%	40		60

SPI Data (GPS_SPI_DATA)

The SPI Data is a bi-directional synchronous serial data signal used to transfer commands and data between the GPS RF ASIC and GPS Baseband ASIC.

Parameter	Units	Min	Typ	Max
Data Rate	MHz		0.5*GPS Clock	
Hi Level	Volts	0.8*Vio		
Lo Level	Volts			0.22*Vio

SPI Enable (GPS_SPI_EN)

The SPI Enable is an active low signal output from the GPS Baseband ASIC used to enable data transfer on the SPI Data signal in conjunction with the SPI clock signal.

Parameter	Units	Min	Typ	Max
Hi Level	Volts	0.8*Vio		
Lo Level	Volts			0.22*Vio

Crystal Oscillator Input (XTAL_IN)

The TCXO provides a sine-wave input to the GPS RF ASIC, which is used for down-conversion, sampling, and producing the GPS clock.

Parameter	Units	Min	Typ	Max
Frequency	MHz	-15 PPM	16.368 MHz	+15 PPM
Level	Volts p-p	0.15		1.0